What is claimed is:

[Claim 1] 1. A method of programming nonvolatile memory (NVM) cells comprising:

a) providing a plurality of NVM cells;

b) providing a variable reference signal, said variable reference signal being varied to one of a plurality of reference levels corresponding to reprogrammed threshold voltages;

c) selecting a state threshold from said plurality of reference levels, the selected said state threshold establishing a logic level threshold; and

d) programming ones of said plurality of NVM cells responsive to said state threshold.

[Claim 2] 2. A method of programming NVM cells as in claim 1, wherein the step (c) of selecting a state threshold comprises programming a dummy NVM cell to a reference threshold level, said reference threshold level being at least at a current programmed cell threshold, said current programmed cell threshold being higher than a current unprogrammed cell threshold.

[Claim 3] 3. A method of programming NVM cells as in claim 1, wherein the step (d) of programming NVM cells comprises:

i) selecting ones of said plurality of NVM cells; and

ii) increasing the cell threshold for selected said ones to a higher cell threshold.

[Claim 4] 4. A method of programming NVM cells as in claim 3, wherein the step (d) of programming NVM cells further comprises:

iii) comparing said selected ones of said plurality of NVM cells against said variable reference signal for an indication that said ones have been programmed; and

iv) returning to step (i) for any of said selected ones not providing said indication.

[Claim 5] 5. A method of programming NVM cells as in claim 4, wherein said NVM cells are included on an integrated circuit (IC) chip and once an upper one of said plurality of reference levels has been provided, an indication is provided that said IC chip should be replaced.

[Claim 6] 6. A method of programming NVM cells as in claim 5, wherein said NVM cells are in logic on said IC chip, whereby said NVM cells are not erased between writes.

[Claim 7] 7. A method of programming NVM cells as in claim 5, wherein said NVM cells are in an array of said NVM cells on said IC chip, whereby said array is not erased between writes.

[Claim 8] 8. A reprogrammable integrated circuit (IC) comprising:

a plurality of nonvolatile storage cells;

a differential sense amplifier, ones of said plurality of nonvolatile storage cells being selectively coupled to a first input of said differential sense amplifier; and

a variable reference signal coupled to a second input of said differential sense amplifier, said variable reference signal having a plurality of selectable reference levels corresponding to reprogrammed cell threshold voltages, wherein with each write cycle a different one of said selectable reference levels is coupled to said second input, contents of said nonvolatile storage cells subsequently being compared by said differential sense amplifier against said different one.

[Claim 9] 9. A reprogrammable IC as in claim 8, further comprising a dummy cell developing said variable reference, said dummy cell having a threshold voltage programmed with each said write cycle at least at a current cell threshold voltage and below a reprogrammed cell threshold voltage.

[Claim 10] 10. A reprogrammable IC as in claim 9, wherein at least one of said plurality of nonvolatile storage cells is embedded in logic on said IC.

[Claim 11] 11. A reprogrammable IC as in claim 9, wherein said IC is a CMOS IC, said nonvolatile storage cells and said dummy cell are n-type field

effect transistor (NFET) floating gate devices, said reprogrammable CMOS IC further comprising:

a load p-type field effect transistor (PFET) loading ones of said plurality of nonvolatile storage cells coupled to said first input of said differential sense amplifier; and

a dummy load PFET loading said dummy cell.

[Claim 12] 12. A reprogrammable CMOS IC as in claim 11, further comprising an array of said nonvolatile storage cells.

[Claim 13] 13. A reprogrammable CMOS IC as in claim 12, wherein said array is a nonvolatile memory array, said IC further comprising:

a word decode partially selecting ones of said plurality of nonvolatile storage cells connected to one of a plurality of word lines; and

a bit decode selectively coupling partially selected said ones to said first input of said differential sense amplifier.

[Claim 14] 14. A reprogrammable IC as in claim 8, wherein at least one of said plurality of nonvolatile storage cells have a programmed cell threshold voltage and remaining ones of said storage cells have an unprogrammed cell threshold voltage below said programmed cell threshold voltage.

[Claim 15] 15. A reprogrammable IC as in claim 9, wherein said remaining ones of said storage cells have one a of a plurality of unprogrammed cell threshold voltages below said programmed cell threshold voltage.

[Claim 16] 16. A reprogrammable CMOS integrated circuit (IC) comprising:

a plurality of nonvolatile storage cells;

a differential sense amplifier, nonvolatile storage cells being coupled to a first input of said differential sense amplifier; and

a variable reference signal coupled to a second input of said differential sense amplifier, said variable reference signal having a plurality of selectable reference levels corresponding to reprogrammed cell threshold voltages,

wherein with each write cycle a different one of said selectable reference levels is coupled to said second input, contents of said nonvolatile storage cells subsequently being compared by said differential sense amplifier against said different one.

[Claim 17] 17. A reprogrammable CMOS IC as in claim 16, further comprising:

an nonvolatile memory array of said nonvolatile storage cells;

a word decode partially selecting ones of said plurality of nonvolatile storage cells connected to one of a plurality of word lines; and

a bit decode selectively coupling partially selected said ones to said first input of said differential sense amplifier.

[Claim 18] 18. A reprogrammable CMOS IC as in claim 17, further comprising:

a dummy cell developing said variable reference, said dummy cell having a threshold voltage programmed with each said write cycle at least at a current cell threshold voltage and below a reprogrammed cell threshold voltage;

an active load device loading ones of said plurality of nonvolatile storage cells coupled to said first input of said differential sense amplifier; and

an active dummy load device loading said dummy cell.

[Claim 19] 19. A reprogrammable CMOS IC as in claim 16, wherein at least one of said plurality of nonvolatile storage cells is embedded in logic on said IC.

[Claim 20] 20. A reprogrammable CMOS IC as in claim 16, wherein at least one of said plurality of nonvolatile storage cells have a programmed cell threshold voltage and remaining ones of said storage cells have a plurality of unprogrammed cell threshold voltages below said programmed cell threshold voltage.